IN THE SPECIFICATION:

Please replace paragraph number **[0010]** with the following rewritten paragraph:

[0010] Several drawbacks exist with conventional die stacking techniques. As shown in FIG. 1, the top semiconductor die 12 of a semiconductor die stack assembly 10 is typically ~~wire bonded~~ bonded with wire bonds 14 to a substrate 16. With wire bonding, the encapsulant 17 must accommodate the wire loops, increasing the overall package height 18. Further, with wire bonding, a chance of electrical performance problems or shorting exists if the various wires loops come too close to each other. The wire loops can also get swept during packaging, causing further electrical problems. Flip chip attachment overcomes some of these limitations. However, die stacking that relies on flip chip attachment requires the stacked die to be manufactured and vertically aligned to bring complementary circuitry into perpendicular alignment with a lower die.

Please replace paragraph number **[0022]** with the following rewritten paragraph:

[0022] FIG. 4 is a partial ~~cross-section~~ cross-sectional view of a redistribution circuit on a semiconductor die;

Please replace paragraph number **[0035]** with the following rewritten paragraph:

[0035] A plurality of discrete conductive elements 28, in the form of the illustrated bond ~~wires 28~~ wires, TAB elements, leads or the like, extend from bond pads 32 (FIG. 3) on the first semiconductor die 20 to contact areas (not shown) of the substrate 30. FIG. 3 depicts a top view of the active surface 22 of the first semiconductor die 20. Thus, components common to FIGs. 2 and 3 retain the same numeric designation. Referring to FIG. 3, the first semiconductor die 20 includes a plurality of bond pads 32 on the active surface 22 thereof, which are connected to integrated circuitry (not shown) of the first semiconductor die 20. In addition, the first semiconductor die 20 includes redistribution circuits 34, each of which includes a first redistribution bond pad 36 and a second redistribution bond pad 38 that is electrically connected to the first redistribution bond pad 36 by way of a conductive trace 37 extending therebetween.

Each first redistribution bond pad 36 is located so as to align with a corresponding bond pad on the active surface 46 of the second semiconductor die 40 (not shown) upon positioning the second semiconductor die 40 in inverted orientation over the first semiconductor die 20. The second redistribution bond pad 38 may be located along the outer periphery of the first semiconductor die 20 to facilitate electrical connection of the second redistribution bond pads 38 to corresponding contact areas (not shown) of the substrate 30.

Please replace paragraph number **[0040]** with the following rewritten paragraph:

[0040] If desired, the stacked semiconductor assembly 100 may be encapsulated with an encapsulating material 70, such as silicone or epoxy, to form an encapsulated stacked semiconductor assembly 100. As seen by comparing FIG. 1 and FIG. 2, by eliminating the need for wire bonds to the top semiconductor die, the overall package height (18, 48) may be reduced. Alternatively, if the package height is maintained, the present invention provides increased protection between the ~~bond wires~~ conductive elements 28 (and backside 74 of second semiconductor die 40) and the edges of the encapsulating material 70. Further, the elimination of long ~~bond wires~~ wire bonds 14 between a top semiconductor die 12 and a substrate 16 results in less static and a decreased chance of wire sweep during packaging. A plurality of external solder balls 72 may be used for electrical connection of the stacked semiconductor assembly 100 to another assembly such as a printed circuit board (not shown).

Please replace paragraph number **[0042]** with the following rewritten paragraph:

[0042] Another embodiment of the invention provides a stacked semiconductor assembly wherein the edges of at least two of the semiconductor ~~diceare~~ dice are not aligned (FIGs. 9, 10, 11). As depicted in FIG. 9, a stacked semiconductor package 900 according to the present invention is provided with a reduced package height 948 or with additional space between electrical connections and the encapsulating material without adding any height to the package. The stacked semiconductor package 900 includes a substrate 930 that includes conductive terminal pads and corresponding traces (not shown) and has at least two

semiconductor dice 920, 940 disposed thereon. At least one of the peripheral edges 964, 966 of the top semiconductor die 940 extends laterally beyond at least one of the peripheral edges 960, 962 of a bottom semiconductor die 920. The top semiconductor die 940 has an active surface 946 facing the active surface 922 of the bottom semiconductor die 920. The bottom semiconductor die 920 may be disposed directly on the substrate 930, as shown, or may be stacked above at least one other die (not shown). Bond pads 936 of the bottom semiconductor die 920 may be electrically connected to the corresponding terminals 968 of the substrate 930, by way of discrete conductive elements 928. An electrical connector 944, such as a pillar column, bump, or ball of conductive material (e.g., solder, other metal, conductive or conductor-filled epoxy, anistropically conductive elastomer, etc.), extends from a bond pad 942 on the active surface 946 of the top semiconductor die 940 to the corresponding terminal pad 974 of the substrate 930. If desired, a layer or film of dielectric or insulative material 926 may be positioned between the active surface 946 of the top semiconductor die 940 and the active surface 922 of the bottom semiconductor die 920. If the stacked semiconductor package 900 is encapsulated, a plurality of external solder balls 972 may be used for electrical connection of the stacked semiconductor package 900 to another assembly such as a printed circuit board (not shown).

Please replace paragraph number **[0043]** with the following rewritten paragraph:

[0043] In the stacked semiconductor package 900, of the embodiment shown in FIG. 9, the active surface 922 of the bottom semiconductor die 920 may include a redistribution circuit as described herein and in FIG. 3. However, if the bond pads 942 of the top semiconductor die 940 can be connected to corresponding terminal pads 974 on the substrate 930 as shown in ~~FIG. 9~~ FIG. 9, a redistribution circuit is not required. Instead, as shown in FIG. 12, the active surface 922 of the bottom semiconductor die 920 may include bond pads 936 that are directly connected to corresponding terminal pads 974 on the substrate 930.

Please replace paragraph number **[0044]** with the following rewritten paragraph:

[0044] The stacked semiconductor package 900″ of FIG. 13 is similar to the stacked semiconductor package 900 depicted in FIG. 9. FIG. 13 shows three stacked semiconductor ~~die,~~ dice, however any number of ~~die~~ dice may be used. A first semiconductor die 950″ may be disposed directly on a substrate 930″, as shown, or may be stacked above at least one other die (not shown). A second semiconductor die 920″ may be disposed above the first semiconductor die 950″ such that the active surface 952″ of first semiconductor die 950″ faces the backside 921″ of second semiconductor die 920″. The first semiconductor die 950″ and second semiconductor die 920″ can be electrically connected to corresponding terminals 968″ on the substrate 930″, by way of discrete conductive elements 928″.

Please replace paragraph number **[0047]** with the following rewritten paragraph:

[0047] The stacked semiconductor package 900‴ of FIG. 14 is similar to the stacked semiconductor package 900 depicted in FIG. 9. The backside 924‴ of bottom semiconductor die 920‴ may be disposed on a substrate 930‴. Alternatively, ~~a one or~~ one or more semiconductor ~~die~~ dice may be disposed between the bottom semiconductor die 920‴ and the substrate 930‴. The bottom semiconductor die 920‴ may be electrically connected to the substrate 930‴ by way of discrete conductive elements 928‴. An insulative layer 926‴ may be disposed between bottom semiconductor die 920‴ and top semiconductor die 940‴. At least one peripheral edge 966‴ of the top semiconductor die 940‴ extends beyond a corresponding peripheral edge 962‴ of the bottom semiconductor die 920‴, and at least one peripheral edge 960‴ of the bottom semiconductor die 920‴ extends beyond a corresponding peripheral edge 964‴ of the top semiconductor die 940‴. A first electrical connector 944‴, such as a pillar column, bump, or ball of conductive material (e.g., solder, other metal, conductive or conductor filled epoxy, anistropically conductive elastomer, etc.), extends from a bond pad 942‴ on the active surface 946‴ of the top semiconductor die 940‴ to its corresponding bond pad 936‴ on the bottom semiconductor die 920‴. The active surface 922‴ of the bottom semiconductor die 920‴ may include a redistribution circuit as depicted in FIG. 3 and described herein. A

second electrical connector 944‴ extends from a bond pad 942‴ on the active surface 946‴ of the top semiconductor die 940‴ to its corresponding terminals 968‴ of the substrate 930‴.

IN THE CLAIMS:

Claims 36-75 and 87-97 were previously canceled herein. Claims 12, 24 and 102 have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (previously presented) A stacked semiconductor assembly, comprising:

a first semiconductor die including an active surface and a backside, said active surface including a plurality of bond pads and at least one redistribution bond pad circuit thereon, said plurality of bond pads electrically connected to integrated circuitry of said first semiconductor die, said at least one redistribution bond pad circuit electrically isolated from said integrated circuitry of said first semiconductor die and including a plurality of redistribution bond pads;

a second semiconductor die including an active surface, a backside, and a plurality of bond pads on said active surface thereof, said active surface of said second semiconductor die facing said active surface of said first semiconductor die; and

at least one electrical connector extending between at least one bond pad of said plurality of bond pads on said active surface of said second semiconductor die and at least one redistribution bond pad of said plurality of redistribution bond pads on said first semiconductor die.

2. (previously presented) The stacked semiconductor assembly of claim 1, wherein said first semiconductor die is disposed on a substrate.

3. (previously presented) The stacked semiconductor assembly of claim 2, wherein said first semiconductor die is electrically connected to said substrate with intermediate conductive elements.

4. (previously presented) The stacked semiconductor assembly of claim 3, wherein said intermediate conductive elements comprise bond wires.

5. (previously presented) The stacked semiconductor assembly of claim 2, wherein said at least one redistribution bond pad circuit comprises a plurality of conductive traces, at least one conductive trace of said plurality of conductive traces connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality of redistribution bond pads, said second redistribution bond pad proximate the perimeter of said first semiconductor die.

6. (previously presented) The stacked semiconductor assembly of claim 5, wherein said second redistribution bond pad is electrically connected to said substrate.

7. (previously presented) The stacked semiconductor assembly of claim 1, wherein peripheral edges of said first semiconductor die and edges of said second semiconductor die are substantially vertically aligned.

8. (previously presented) The stacked semiconductor assembly of claim 1, wherein said second semiconductor die is smaller than said first semiconductor die.

9. (previously presented) The stacked semiconductor assembly of claim 1, wherein said at least one electrical connector spaces the active surface of said second semiconductor die from the active surface of said first semiconductor die.

10. (previously presented) The stacked semiconductor assembly of claim 1, further comprising a substrate under said first semiconductor die, said substrate including a plurality of contact areas thereon.

11. (previously presented) The stacked semiconductor assembly of claim 10, wherein at least one bond pad of said plurality of bond pads on said first semiconductor die is electrically connected to a corresponding contact area of said plurality of contact areas on said substrate.

12. (currently amended) The stacked semiconductor assembly of claim 10, wherein said at least one redistribution bond pad of said at least one redistribution bond pad circuit is electrically connected to a corresponding contact area of said plurality of contact areas on said substrate.

13. (previously presented) The stacked semiconductor assembly of claim 10, further comprising at least one semiconductor die vertically stacked on said substrate, wherein said backside of said first semiconductor die is located above said at least one stacked semiconductor die.

14. (previously presented) The stacked semiconductor assembly of claim 1, further comprising an insulative layer between said first semiconductor die and said second semiconductor die.

15. (previously presented) The stacked semiconductor assembly of claim 14, wherein said insulative layer comprises an adhesive material.

16. (previously presented) The stacked semiconductor assembly of claim 1, wherein said at least one electrical connector comprises a substantially columnar pillar.

17. (previously presented) The stacked semiconductor assembly of claim 16, wherein said substantially columnar pillar is copper.

18. (previously presented) The stacked semiconductor assembly of claim 1, wherein said at least one electrical connector comprises a solder ball.

19. (previously presented) The stacked semiconductor assembly of claim 1, wherein at least one peripheral edge of said second semiconductor die extends laterally beyond at least one corresponding peripheral edge of said first semiconductor die.

20. (previously presented) The stacked semiconductor assembly of claim 19, further comprising at least one electrical connector extending from at least one bond pad of said plurality of bond pads on said second semiconductor die and a corresponding contact area of a substrate.

21. (previously presented) The stacked semiconductor assembly of claim 1, wherein at least one peripheral edge of said first semiconductor die extends laterally beyond at least one corresponding peripheral edge of said second semiconductor die.

22. (previously presented) A semiconductor assembly, comprising:

a substrate;

a first semiconductor die including an active surface, a second surface, and a plurality of peripheral edges, said second surface disposed on said substrate, said active surface having a plurality of bond pads thereon;

a second semiconductor die including an active surface, a second surface, a plurality of peripheral edges and a plurality of bond pads on said active surface, said active surface of said second semiconductor die facing said active surface of said first semiconductor die, at least one bond pad of said plurality of bond pads of said first semiconductor die communicating with a corresponding redistribution circuit of said second semiconductor die, said redistribution circuit being electrically isolated from integrated circuitry of said second semiconductor die, at least one edge of said plurality of peripheral edges of said

second semiconductor die extending laterally beyond at least one corresponding peripheral edge of said plurality of peripheral edges of said first semiconductor die; and at least one connective element extending from at least one bond pad of said plurality of bond pads on said active surface of said second semiconductor die to a corresponding contact area of said substrate adjacent to said at least one corresponding peripheral edge of said first semiconductor die.

23. (original) The semiconductor assembly of claim 22, further comprising at least one additional semiconductor die stacked vertically between said first semiconductor die and said second semiconductor die.

24. (currently amended) The semiconductor assembly of claim 23, wherein said at least one additional semiconductor die and said first semiconductor die ~~are all~~ are electrically connected to said substrate by discrete conductive elements.

25. (previously presented) The semiconductor assembly of claim 23, wherein a third semiconductor die of said at least one additional semiconductor die is disposed directly below said second semiconductor die, said third semiconductor die including an active surface and a backside, said active surface including a plurality of bond pads and at least one redistribution bond pad circuit thereon, said plurality of bond pads of said third semiconductor die electrically connected to integrated circuitry of said third semiconductor die, said at least one redistribution bond pad circuit independent from the integrated circuitry of said third semiconductor die and including a plurality of redistribution bond pads.

26. (original) The semiconductor assembly of claim 25, wherein said at least one redistribution bond pad circuit comprises a plurality of conductive traces, at least one conductive trace of said plurality of conductive traces connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality of

redistribution bond pads, said second redistribution bond pad proximate the perimeter of said third semiconductor die.

27. (previously presented) The semiconductor assembly of claim 26, wherein at least one connective element extends between said least one bond pad on said active surface of said second semiconductor die and said first redistribution bond pad on said active surface of said third semiconductor die.

28. (original) The semiconductor assembly of claim 27, wherein said second redistribution bond pad is electrically connected to said substrate by discrete conductive elements.

29. (original) The semiconductor assembly of claim 24, wherein said discrete conductive elements comprise at least one of wire bonds, TAB elements, and leads.

30. (previously presented) The semiconductor assembly of claim 22, wherein said at least one connective element comprises a substantially columnar pillar.

31. (original) The semiconductor assembly of claim 30, wherein said substantially columnar pillar is copper.

32. (original) The semiconductor assembly of claim 22, wherein said at least one connective element comprises a solder ball.

33. (original) The semiconductor assembly of claim 22, wherein said at least one connective element extends from said at least one bond pad of said second semiconductor die to said corresponding contact area of said substrate.

34. (original) The semiconductor assembly of claim 22, further comprising an insulative layer between said first semiconductor die and said second semiconductor die.

35. (original) The semiconductor assembly of claim 34, wherein said insulative layer comprises an adhesive material.

Claims 36 - 75 (canceled)

76. (previously presented) A semiconductor device for use in a stacked semiconductor assembly, said semiconductor device comprising:
a backside;
an active surface including a plurality of bond pads; and
at least one redistribution bond pad circuit on said active surface, said at least one redistribution bond pad circuit electrically isolated from integrated circuitry of said semiconductor device.

77. (previously presented) The semiconductor device of claim 76, wherein said plurality of bond pads is electrically connected to said integrated circuitry of said semiconductor device.

78. (previously presented) The semiconductor device of claim 77, wherein said plurality of bond pads is centrally located on said active surface.

79. (previously presented) The semiconductor device of claim 77, wherein said plurality of bond pads is located proximate the perimeter of said active surface.

80. (previously presented) The semiconductor device of claim 76, wherein said at least one redistribution bond pad circuit comprises a first redistribution bond pad electrically connected to a second redistribution bond pad.

81. (previously presented) The semiconductor device of claim 80, wherein said at least one redistribution bond pad circuit further comprises a conductive trace extending between said first redistribution bond pad and said second redistribution bond pad.

82. (original) The semiconductor device of claim 81, wherein said conductive trace comprises at least one of titanium, copper, aluminum, NiV and nickel.

83. (original) The semiconductor device of claim 80, wherein said first redistribution bond pad is located on said active surface in a location that mirrors a location of a corresponding bond pad of a second semiconductor device to be positioned above said semiconductor device.

84. (original) The semiconductor device of claim 83, wherein said second redistribution bond pad is proximate the perimeter of said semiconductor device.

85. (original) The semiconductor device of claim 80, wherein said first redistribution bond pad is electrically connected to a corresponding bond pad on an active surface of a second semiconductor device.

86. (original) The semiconductor device of claim 85, wherein said second redistribution bond pad is electrically connected to a contact area on a substrate.

Claims 87 - 97 (canceled)

98. (previously presented) A semiconductor assembly, comprising:

a substrate;

a first semiconductor die including an active surface, a second surface, and a plurality of peripheral edges, said second surface disposed on said substrate, said active surface having a plurality of bond pads thereon;

a second semiconductor die including an active surface, a second surface, a plurality of peripheral edges and a plurality of bond pads on said active surface, said active surface of said second semiconductor die facing said active surface of said first semiconductor die, at least one edge of said plurality of peripheral edges of said second semiconductor die extending laterally beyond at least one corresponding peripheral edge of said plurality of peripheral edges of said first semiconductor die;

a third semiconductor die disposed directly below said second semiconductor die, said third semiconductor die including an active surface and a backside, said active surface including a plurality of bond pads and at least one redistribution bond pad circuit thereon, said plurality of bond pads of said third semiconductor die electrically connected to integrated circuitry of said third semiconductor die, said at least one redistribution bond pad circuit independent from the integrated circuitry of said third semiconductor die and including a plurality of redistribution bond pads; and

at least one connective element extending from at least one bond pad of said plurality of bond pads on said active surface of said second semiconductor die to a corresponding contact area of said substrate adjacent to said at least one corresponding peripheral edge of said first semiconductor die.

99. (previously presented) The semiconductor assembly of claim 98, wherein said at least one redistribution bond pad circuit comprises a plurality of conductive traces, at least one conductive trace of said plurality of conductive traces connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality

of redistribution bond pads, said second redistribution bond pad proximate the perimeter of said third semiconductor die.

100. (previously presented) The semiconductor assembly of claim 99, wherein at least one connective element extends between said least one bond pad on said active surface of said second semiconductor die and said first redistribution bond pad on said active surface of said third semiconductor die.

101. (previously presented) The semiconductor assembly of claim 100, wherein said second redistribution bond pad is electrically connected to said substrate by discrete conductive elements.

102. (currently amended) The semiconductor assembly of claim ~~98~~ 101, wherein said discrete conductive elements comprise at least one of wire bonds, TAB elements, and leads.

103. (previously presented) The semiconductor assembly of claim 98, wherein said at least one connective element comprises a substantially columnar pillar.

104. (previously presented) The semiconductor assembly of claim 103, wherein said substantially columnar pillar is copper.

105. (previously presented) The semiconductor assembly of claim 98, wherein said at least one connective element comprises a solder ball.

106. (previously presented) The semiconductor assembly of claim 98, wherein said at least one connective element extends from said at least one bond pad of said second semiconductor die to said corresponding contact area of said substrate.

107. (previously presented) The semiconductor assembly of claim 98, further comprising an insulative layer between said first semiconductor die and said second semiconductor die.

108. (previously presented) The semiconductor assembly of claim 107, wherein said insulative layer comprises an adhesive material.

REMARKS

This amendment corrects errors in the text. Entry is respectfully solicited. No new matter has been added.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,

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